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MOSCONE WEST CENTER  
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# Innovative High-Voltage Interfaces in Standard Logic Processes for Enhanced Sensor Applications

Stephen Fairbanks, CEO and CTO, Certus

Pradeep Thiagarajan, Principal Product Manager, Siemens

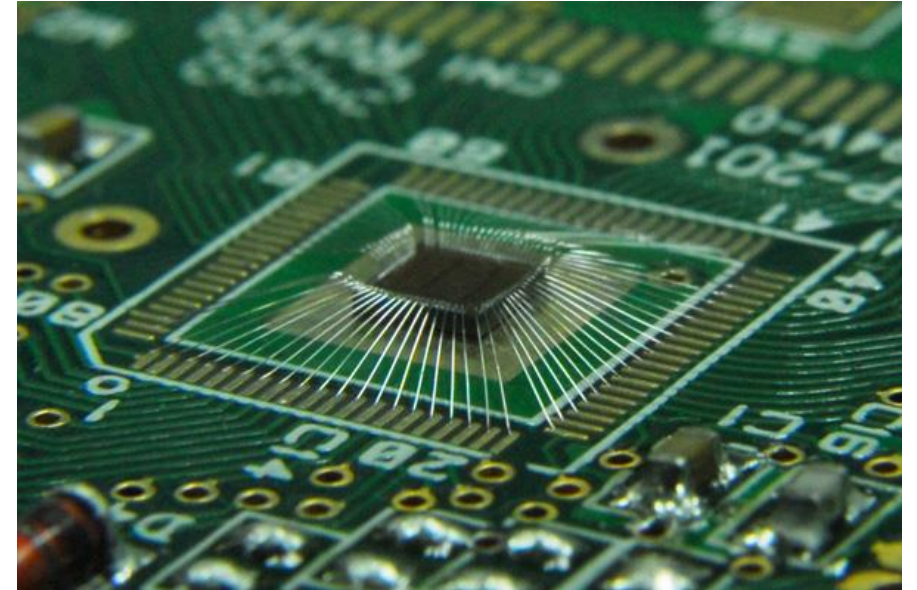
Lih-Jen Hou, Technical Product Manager, Siemens



# Motivation

## Emerging trends of combining logic process and High Voltage (HV) sensors in one design

- Mobile, IoT and AI applications pursue **flexibility** and **capability**
- MEMS and RF components are adopted in the applications, requires **additional discrete components** to achieve high-voltage domain
- Fully-integrated chips of compact design require **HV interface in logic process**

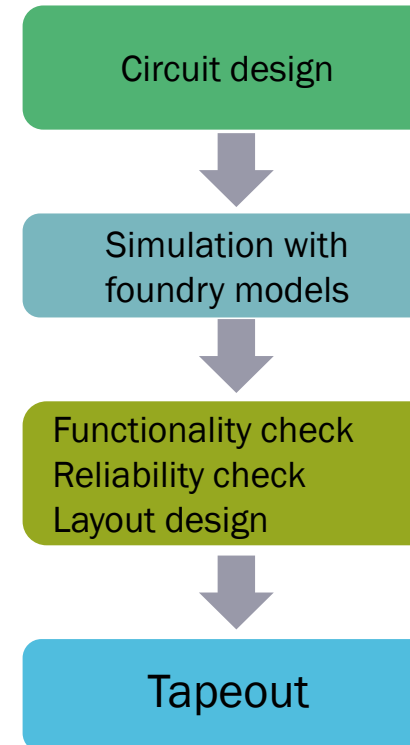


# Motivation

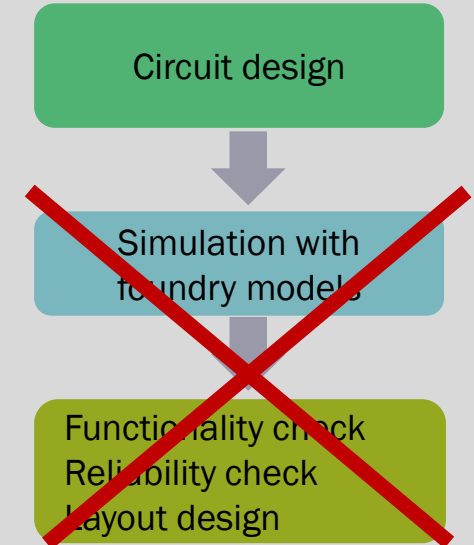
## Handling high-voltage processes alongside logic devices adds complexity

- Device over-voltage stresses on purpose commonly raise **reliability concerns**
- Simulations are inaccessible due to the scenario is **out-of-spec of the designed model** for **reliability concerns**, including ESD
- **Several iterations** are needed to complete the design phase
- **Custom symbols/schematics** to pass LVS is necessary

### Conventional Flow



### HV + Logic Process Flow



- Existing model is **out of scope**
- **Unable to proceed DRC/LVS** due to lack of usable model
- No previous data for building stable circuits aiming for fixing reliably items

# Main Idea

## Silicon proven High-Voltage RF switch

- Process: 40nm logic process
- Voltage range: -18V to 25V
- ESD testing: Qualified for 2kV HBM and 500V CDM
- I-V curve performance: Low leakage verified between -18V~39V with the applied voltage
- Leakage performance: Nominal leakage consistently <100pA, nearly undetectable by certified instrument
- Applications: RF, MEMS, analog sensors, PMIC

Table 1: HV RF Switch Electrical Parameters

Parameter	Description	Min	Typ	Max	Unit
$V_{NOM}$	Normal Operation Range	-18		25	Volt
$V_{ctrl}$	Input Control Pin (High Assertion)	0		1.32	Volt
$R_{on}$	ON-Resistance when $V_{ctrl}$ is asserted	650	850	965	Ohms
$V_{TN}$	Negative Trigger Voltage		-18.5	-18	Volt
$V_{TP}$	Positive Trigger Voltage, Avalanche Point	31	33	35	Volt
$V_{HOLD}$	High Holding Voltage (at targeted 2kV HBM Current)	38	42	44	
$I_{in}$	Input Leakage (when switch is off)		100p	1	nA
$T_j$	Junction Temperature	-40		125	C
$C_{Load}$	Capacitive Load		1.5p	2p	pF
$I_{esd}$	Maximum ESD Current Handling			1.45	A
HBM	HBM ESD Rating	2			kV
CDM	CDM ESD Rating	500			V

Representative parameters of HV RF switch

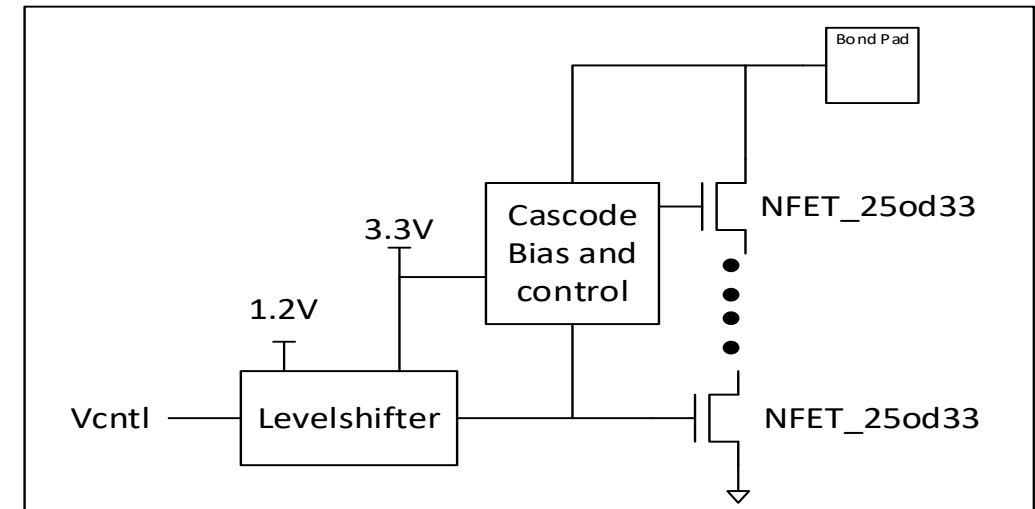


Diagram of HV RF switch by logic process



# Main Idea

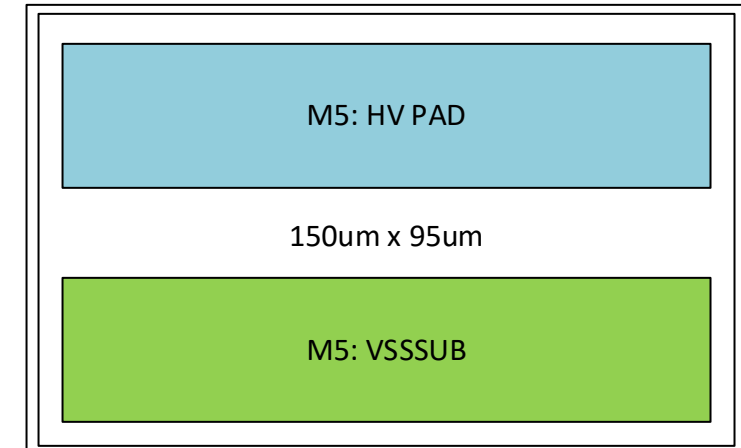
## Silicon proven ESD design

- **Process:** 40nm logic process
- **Voltage range:** -18V to 30V
- **ESD testing:** Qualified for 2kV HBM and 500V CDM
- **Pad configuration:** Propriety configuration of pad design enables HV capability on ESD with logic process
- **Applications:** High-voltage audio applications, NFC
  - Actual use case with NFC to have on-board HV ESD solution for its capability of -18V~30V voltage range

Table 1: Electrical Parameters

Parameter	Description	Min	Typ	Max	Unit
V <sub>NOM</sub>	Normal Operation Range	-18*		30	Volt
V <sub>TN</sub>	Negative Trigger Voltage		-20	-18	Volt
V <sub>TP</sub>	Positive Trigger Voltage, Avalanche Point	30	35	na	Volt
V <sub>HOLD</sub>	High Holding Voltage (at targeted 2kV HBM Current)	30	35	na	
I <sub>in</sub>	Input Leakage		0.1	1	nA
T <sub>j</sub>	Junction Temperature	-40		125	C
C <sub>Load</sub>	Capacitive Load		2p	2.5p	pF
I <sub>esd</sub>	Maximum ESD Current Handling			1.5	A
HBM	HBM ESD Rating	2			kV
CDM	CDM ESD Rating	500			V

Representative parameters of HV ESD

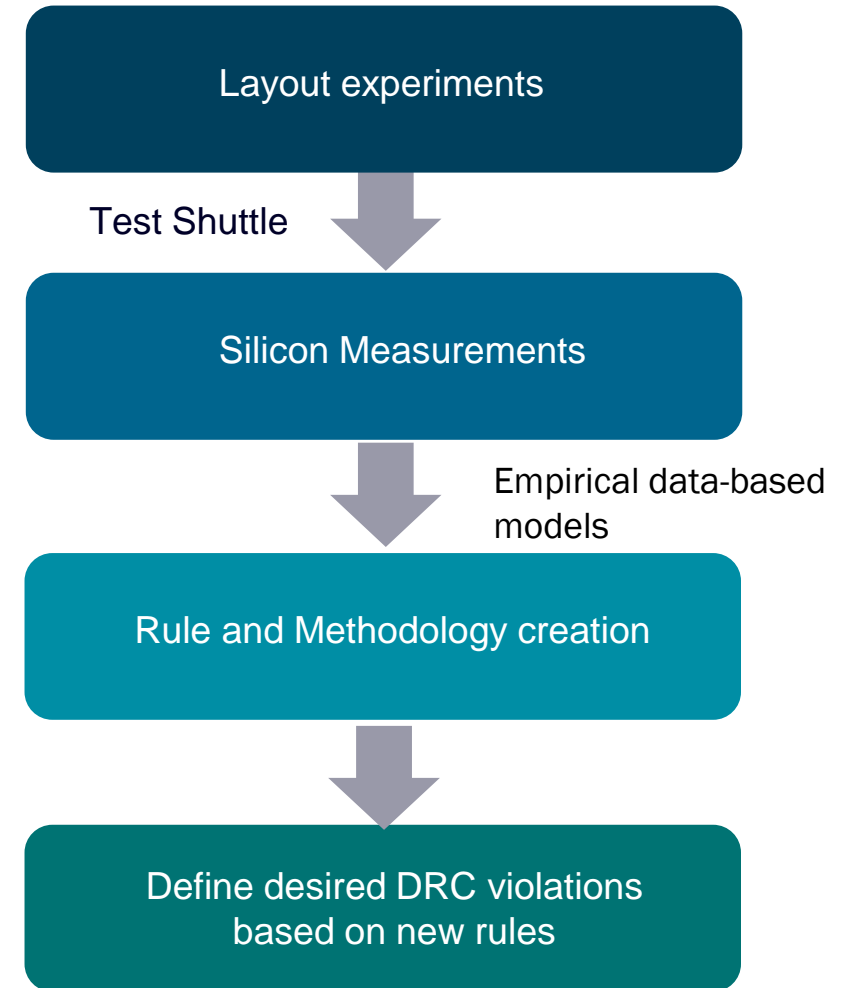


Pad configuration of HV ESD by logic process

# Main Idea

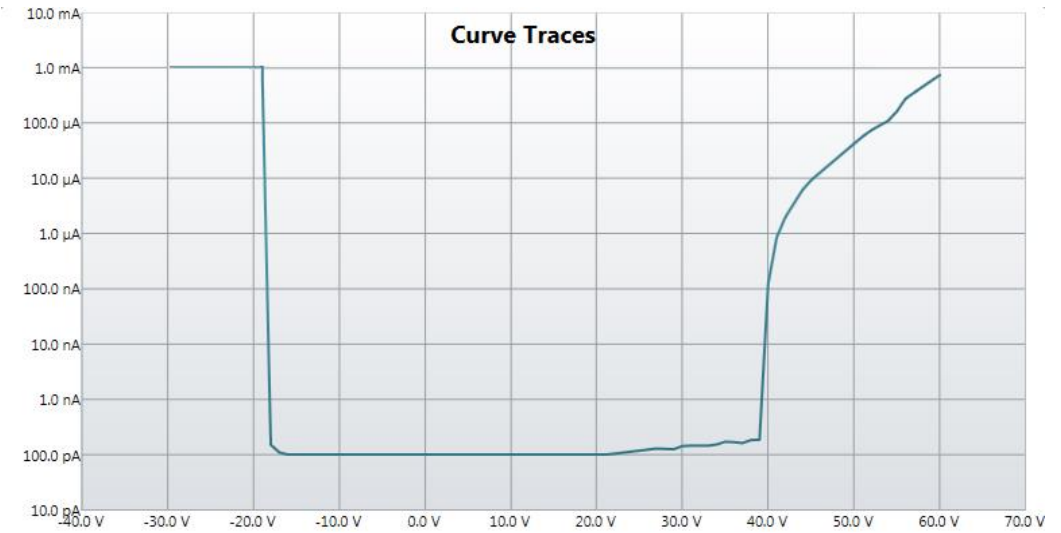
Development of HV RF switch and ESD on logic process is empirical

1. Initial test chip is required for a new development process
2. Tuning new HV structures in the process based on single test chip data based on the
3. DRC violations are required to use for verifying new designs
4. Generate dedicated end-user LVS and simulation models with **Siemens' Calibre® nmPlatform** and **Siemens Analog FastSPICE (AFS)**, part of **Solido™ Simulation Suite**

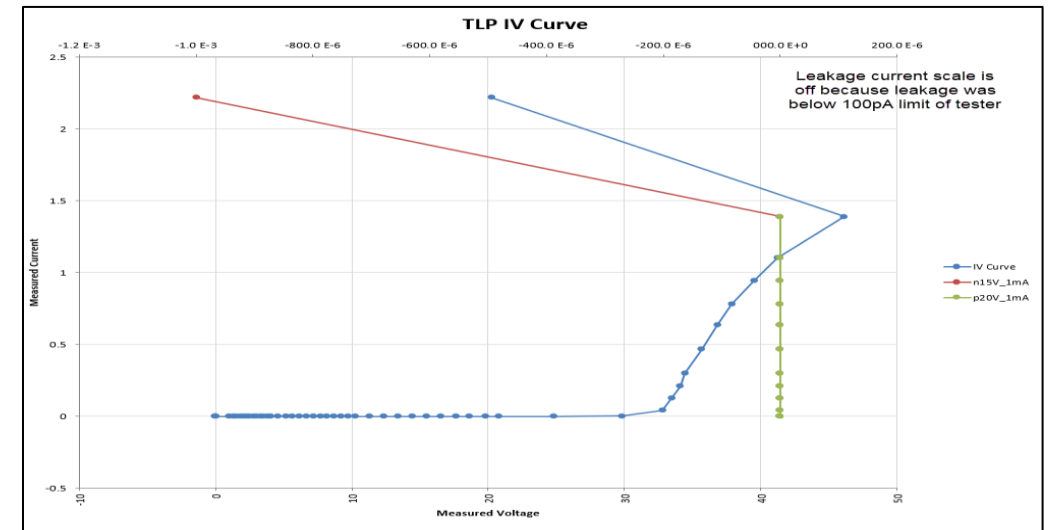


# Evidence

- HV RF switch shows significant on/off behavior **between  $>-18V$  and  $>25V$**  based on silicon measurement result(I-V curve)
- TLP I-V curve on silicon measurement result shows
  - The logic process based ESD design can sustain under  **$30V$  voltage/ $1mA$  current injection** with tiny leakage current even it's in breakdown region
  - Certus's ESD devices can hold till  **$\sim 45V$**  until the breakdown



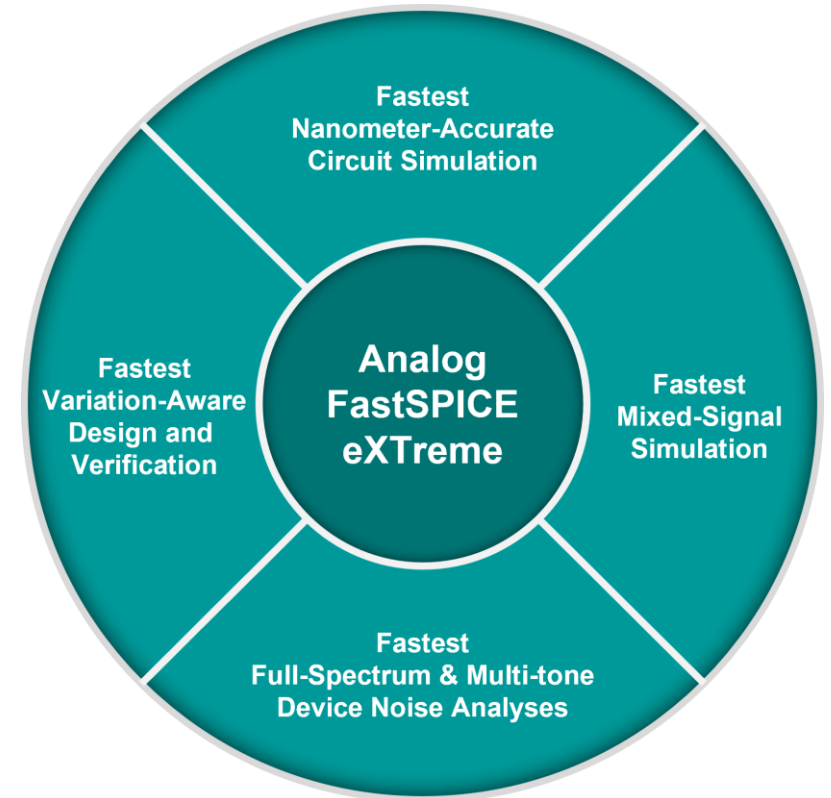
I-V curve of HV RF switch with on/off mode



TLP I-V curve for ESD verification

# Evidence

- Designing test chip for HV RF switch and ESD require to run simulations with the following tools, for getting the initial data:
  - **Calibre DRC, LVS:** For creating customized DRC/LVS model
  - **Calibre xACT and PEX Extraction:** For accurate simulation with post-net
  - **Analog FastSPICE:** DC/AC/Transient simulation
- AFS for analog verification provides significant performance gains without compromising accuracy, **provide the best solution for Certus's design flow with empirical iteration**





# Summary

- Emerging trends include compact designs that combine logic processes and **high-voltage sensors with complicated design** challenge including
  - Over-stress on logic process
  - Reliability concerns
  - Difficulty of performing simulation
- Certus Semiconductor's HV RF switch and ESD shows the possibility and capability of **implementing HV element on general logic process**
- Certus Semiconductor's successfully builds a design flow by leveraging test chip data in the early phase for embedded HV element
- Siemens EDA is essential for Certus Semiconductor new IO's portfolio design & verification
  - **Analog FastSPICE simulator, part of Solido™ Simulation Suite** for circuit simulation
  - **Calibre DRC, LVS, xACT and PEX** for physical verification and extraction